What is claimed is:

1. An integrated circuit device formed, comprising:
a substrate, including:
a dielectric layer;
a semiconductor layer formed over the dielectric layer;
a first active region formed in the semiconductor layer;
a second active region formed in the semiconductor layer;
a trench formed in the substrate and interposed between the first active region and the second active region; and
wherein the trench contains cells of gaseous components.

2. The integrated circuit device of claim 1, wherein the trench contains a fill material selected from the group consisting of a foamed polymeric material, a cured aerogel and an air gap.

3. The integrated circuit device of claim 2, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of methylsilsesquioxane, polyimides and polynorbornenes.

4. The integrated circuit device of claim 2, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of Type I and Type III polyimides.

5. The integrated circuit device of claim 1, wherein the semiconductor layer includes a silicon layer.

6. The integrated circuit device of claim 1, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

7. The integrated circuit device of claim 1, wherein the dielectric layer includes an air gap.

8. The integrated circuit device of claim 1, wherein the trench extends to a level of the dielectric layer of the substrate.

9. The integrated circuit device of claim 1, wherein the trench extends at least partially into a level of the dielectric layer of the substrate.

10. An integrated circuit device, comprising:
a substrate, including:
a dielectric layer;
a semiconductor layer formed over the dielectric layer;
a first active region formed in the semiconductor layer;
a second active region formed in the semiconductor layer;
a trench formed in the substrate and interposed between the first active region and the second active region; and
wherein the trench is filled with a foamed polymeric material.

11. The integrated circuit device of claim 10, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of methylsilsesquioxane, polyimides and polynorbornenes.

12. The integrated circuit device of claim 10, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of Type I and Type III polyimides.

13. The integrated circuit device of claim 10, wherein the semiconductor layer includes a silicon layer.

14. The integrated circuit device of claim 10, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

15. The integrated circuit device of claim 10, wherein the dielectric layer includes an air gap.

16. An integrated circuit device, comprising:
a substrate, including:
a dielectric layer;
a semiconductor layer formed over the dielectric layer;
a first active region formed in the semiconductor layer;
a second active region formed in the semiconductor layer;
a trench formed in the substrate and interposed between the first active region and the second active region; and
wherein the trench is filled with a cured aerogel.

17. The integrated circuit device of claim 16, wherein the semiconductor layer includes a silicon layer.

18. The integrated circuit device of claim 16, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

19. The integrated circuit device of claim 16, wherein the dielectric layer includes an air gap.

20. An integrated circuit device, comprising:
a substrate, including:
a dielectric layer;
a semiconductor layer formed over the dielectric layer;

a first active region formed in the semiconductor layer;

a second active region formed in the semiconductor layer;

a trench formed in the substrate and interposed between the first active region and the second active region; and

wherein the trench is filled with an air gap.

21. The integrated circuit device of claim 20, wherein the semiconductor layer includes a silicon layer.

22. The integrated circuit device of claim 20, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

23. The integrated circuit device of claim 20, wherein the dielectric layer includes an air gap.

24. An integrated circuit device, comprising:

a substrate, including:

a dielectric layer;

a semiconductor layer formed over the dielectric layer;

a first transistor formed in the semiconductor layer;

a second transistor formed in the semiconductor layer; and

a trench formed in the substrate and interposed between the first transistor and the second transistor, wherein the trench contains cells of gaseous components.

25. The integrated circuit device of claim 24, wherein the trench contains a fill material selected from the group consisting of a foamed polymeric material, a cured aerogel and an air gap.

26. The integrated circuit device of claim 25, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of methylsilsesquioxane, polyimides and polynorbornenes.

27. The integrated circuit device of claim 24, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

28. The integrated circuit device of claim 24, wherein the dielectric layer includes an air gap.

29. A memory system, comprising:
a substrate, including:
a dielectric layer;
a semiconductor layer formed over the dielectric layer;
a first number of transistors formed in the semiconductor layer;
a second number of transistors formed in the semiconductor layer;
a trench formed in the substrate and interposed between the first number of transistors and the second number of transistors; and
wherein the trench contains cells of gaseous components.

30. The memory system of claim 29, wherein the trench contains a fill material selected from the group consisting of a foamed polymeric material, a cured aerogel and an air gap.

31. The memory system of claim 29, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of methylsilsesquioxane, polyimides and polynorbornenes.

32. The memory system of claim 29, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

33. The memory system of claim 29, wherein the dielectric layer includes an air gap.

34. A computer system, comprising:

a memory system, including:

a substrate, including:

a dielectric layer;

a semiconductor layer formed over the dielectric layer;

a first active region formed in the semiconductor layer;

a second active region formed in the semiconductor layer;

a trench formed in the substrate and interposed between the first active region and the second active region, wherein the trench contains cells of gaseous components; and

a processor coupled to the first and second electronic devices.

35. The computer system of claim 34, wherein the trench contains a fill material selected from the group consisting of a foamed polymeric material, a cured aerogel and an air gap.

36. The computer system of claim 35, wherein the foamed polymeric material comprises a polymeric material selected from the group consisting of methylsilsesquioxane, polyimides and polynorbornenes.

37. The computer system of claim 34, wherein the dielectric layer includes a silicon dioxide (SiO_2) layer.

38. The computer system of claim 34, wherein the dielectric layer includes an air gap.